MODELING AND SIMULATION OF FinFET SRAM FOR NANO SCALE DEVICES

D. Sathya¹, N. Logeshwari², M. Devisuriya³
Assistant professor¹, Assistant professor², Assistant professor³

Department of Electronics and Communication Engineering,
Maha Barathi Engineering College,
Chinnasalem,
Tamilnadu, India.
dsathyaece@gmail.com, logeshgupta@gmail.com, suryaece11@gmail.com

ABSTRACT- Sub-threshold leakage and process-induced variations in bulk-Si technology limit the scaling of SRAM into sub-32 nm nodes. New device architectures are being considered to improve control $V_t$ and reduce short channel effects. Among the likely candidates, FinFETs are the most attractive option because of their good scalability and possibilities for further SRAM performance and yield enhancement through independent gating. In this work, low power and robust 6T SRAM cell using FinFET has been proposed. When SRAM is in idle mode, leakage power is reduced by the cells which are based on the $V_t$-control of the cross-coupled inverters of the SRAM cell. This scheme also results in increased Static Noise Margin (SNM) and low standby power consumption. HSPICE simulations for 32 nm FinFET technology is used for analyzing the efficiency. The results show considerable improvements in terms of the standby power as well as read SNM.

Keywords-FinFET, SRAM, low power, design, double gate devices

INTRODUCTION

SRAM arrays are the most important part of the chip in many of digital systems which are implemented by MOSFET transistors. One of two important challenges of scaling the conventional six-transistor (6-T) SRAM cells are the increased transistor leakage and the parameter variation present in the standard CMOS technologies. The gate length scaling increases the device leakage exponentially across technology generations. Additionally, the cell stability will start degrading with decreasing the system supply voltage (VDD) and the transistor threshold voltage ($V_t$) in nanometer technology nodes. The FinFET transistor structure has been introduced as an alternative to the bulk-Si MOSFET structure for improved scalability. The structure has two gates which can be electrically isolated and have two different voltages (back
gate) for an improved operation. For switching the FinFET on/off, the two gates are connected together in double-gate (DG) and they are biased independently in back-gate (BG) mode. The feature of back-gate mode can be used to improve the SRAM cell.

The overall power of a processor depends greatly on large embedded SRAM arrays. The power consumption in an SRAM array consists of a short active time and a very long idle time making the standby power consumption as a major issue. Hence the leakage reduction in large memory array is a major objective for low-power VLSI applications. The cell leakage is commonly suppressed by using a higher transistor threshold voltage.

Read margin can also be improved by utilizing a higher transistor threshold voltage and back-gate biasing helps to control the threshold voltage. In this work, a low power and robust FinFET-based SRAM cell is proposed. The SRAM cells are compared in terms of the static power dissipation, leakage power and average power consumption.

**6T SRAM DESIGN TRADEOFFS**

The important properties of a 6T SRAM are the functionality and density of a memory array. Device sizing and supply voltage determines the functionality by the selection of transistor threshold voltages.

**Area Vs Yield**

SRAM is a commonly used memory element. It stores the data value and its complement. Both storage nodes are statically tied to either \( V_{dd} \) or ground. To achieve this, two inverters are cross-coupled and the output of each inverter is the input of the other inverter. Since two cross-coupled inverters are simply a ring oscillator with two inverters, the storage nodes will settle in stable state. Each storage node is also tied to another transistor, often referred to as “access transistor”. The read or write into the storage node is done by the access transistor. This conventional six transistor setup is known as 6T SRAM cell. A schematic of a 6T SRAM cell is shown in figure 1.
Figure 1. CMOS based SRAM design

The memory device can perform the following actions: hold, read and write. The operation performed by SRAM is examined in connection to Figure 1.

**Hold**: When a SRAM is not written or read, it is in the “hold” state. The wordline (WL) voltage is 0 so both access transistors (AXL and AXR) are turned off. The SRAM is now simply a two-transistor ring oscillator. It is easy to see that the storage nodes (VL and VR) “lock” each other to either of the supply rails voltage (VDD or Ground). Deviations from the supply rail voltage will be eliminated.

**Read**: Before reading a value from the storage nodes, both bitlines (BL) are pre-charged to VDD. The wordline is then turned on. The storage node that stores a 1 will stay at 1 since it is connected to a pre-charged bit line. The storage node that stores a 0 will jump to an intermediate voltage because there is now a current path from the bit line to ground. The intermediate voltage is determined by voltage dividers constructed by one of the access transistors and a NMOS (NL or NR) of the inverters. Since the storage nodes are coupled, the intermediate voltage is not supposed to jump too high, otherwise it will invert the data stored at the storage node (it would be a write operation). Hence, NMOS of the inverters are made larger than the access transistor to ensure that the intermediate voltage does not flip the content of the other storage node.

**Write**: Before writing a value, BLC will be asserted to a value desired to be written while before writing a value, BL on Q side will be asserted to value desired to be written while BL will be asserted to a value opposite to the value to be written. If a 0 is desired to be written, then BLC will be asserted to 0 and BL will be asserted to 1. At the instant when the word line is turned on, the storage node VL will jump to an intermediate voltage as in the read case. The write operation has to be performed through the side with storage node at VDD and bit-line precharged to 0.

**Power**

Large embedded SRAM arrays occupy a major portion of the total power of an processor. Power consumption in an SRAM array consists of short active periods and very long idle periods. Standby power consumption is a major issue in large arrays.

Hence, leakage reduction in large memory arrays has become necessary for low-power VLSI applications. Longer channel lengths or higher transistor threshold voltages can be used to suppress cell leakage. Employing longer channel lengths negatively influence the cell area and also have a particular characteristic of increasing WL and BL capacitances thereby increasing access time and active power. So, longer channel lengths are used moderately. Effective use of higher transistor threshold voltages also negatively influences the access time due to the lower read current. However they improve the read and write margins. Increase in threshold voltage of the NMOS transistors influence the trip voltage resulting in larger read and write margins.
So far discussed how a SRAM cell works. However, a SRAM cell cannot function by itself; it is supported by various peripheral circuits shown in figure 2.

Pre-charge circuit is responsible for pre-charging bit lines to appropriate voltages for reading and writing operation. Decoder controls which row of the SRAM array (a collection of many SRAM cells) should be accessed. Sense amplifier determines the logical value as well as restores voltage swing of bit lines. A MUX is used to select the output of the appropriate SRAM cell.

**Challenges for scaling Bulk-Si SRAM**

The scaling of the classical bulk-Si MOSFET structure down into the sub-20 nm regime requires heavy channel doping to control short channel effects and heavy super-halo implants for sub-surface leakage current control which results in severe degradation of carrier mobilities and high electric field in the ON state. The increased depletion charge density results in a larger depletion capacitance hence a larger sub-threshold slope. $V_t$ variability caused by random dopant fluctuations is another concern for nanoscale bulk-Si MOSFETs.

Designing large arrays requires design for 5 or more standard deviations. Increasing transistor sizes is the fundamental reason for scaling. Segmentation is commonly used to speed up arrays.
A SRAM cell built with bulk CMOS is considered in previous discussions. If FinFETs are available, it is easy to convert bulk CMOS SRAM into FinFET SRAM by simply replacing each NMOS with NFinFET and PMOS with PFinFET. A schematic of a 6T FinFET SRAM cell is shown in figure 3.

FinFET was invented to solve some problems caused by technology scaling, such as short channel effects. Unlike conventional bulk silicon MOSFET, FinFET is a double-gate device, which implies the ability to control the conduction channel front two gates instead of one. The advantages include better leakage power suppression, standby power reduction and compatibility with many existing circuit design methodologies. The simplest case is simply replacing all MOSFET with FinFET in any circuit schematic, and tying the back gate to appropriate voltage to reduce leakage power.

**PROPOSED FinFET SRAM DESIGN**

**Proposed SRAM cell based on FinFET SRAM cells**

The cell shown in Figure 1 is the conventional MOSFET SRAM cell. For this cell, in the standby mode, three of devices have the sub-threshold leakage. That is, when \( V_L = V_{DD} \) and \( AR = 0 \), the transistors with the sub-threshold leakage are the right access transistor, left pull-down transistor and right pull-up transistor. The sub-threshold leakage can be decreased by increasing the threshold voltage. This can be achieved by using the back-gate of the FinFET. The FinFET SRAM cells, proposed in this work, use the back-gate of the FinFET to decrease the standby power consumption and improve the stability of the cell.

![Figure 3: FinFET based SRAM design](image-url)

The cells in figure shows the proposed SRAM cell based on FinFET whose back-gate can be controlled by a voltage other than the front-gate voltage. Connecting the back-gate of the
access transistor to the adjacent bit-cell storage node weakens the access transistor current. This increases the cell stability using a built-in feedback. It does not have a significant effect on the static power because it reduces the threshold voltage of the access transistor with $V_{ds}=0$ in standby mode.

**FinFET structure and Characteristics**

For the HSPICE simulations, 45nm and 32nm gate lengths FinFET technology were used for the transistors used in the SRAM cells. Symmetrical double gate FinFET is used in simulations. To achieve a compact layout area, single-fin for the pull-up and the access transistors in the SRAM bit-cell are considered. The optimum number for 32nm technology is 1 fin and for 45nm technology is 2 fins.

### Table 1: Device Parameters used in Simulations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>32</th>
<th>45</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_G$(nm)</td>
<td>32</td>
<td>45</td>
</tr>
<tr>
<td>$T_{ox}$(A)</td>
<td>14</td>
<td>15</td>
</tr>
<tr>
<td>$T_{si}$(nm)</td>
<td>8.6</td>
<td>8.4</td>
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<tr>
<td>$V_{DD}$(V)</td>
<td>0.9</td>
<td>1</td>
</tr>
<tr>
<td>$N_{BODY}$(#/cm$^{-3}$)</td>
<td>2e16</td>
<td>2e16</td>
</tr>
<tr>
<td>$H_{fin}$(nm)</td>
<td>40</td>
<td>60</td>
</tr>
<tr>
<td>$V_{t0,nmos}$(V)</td>
<td>0.29</td>
<td>0.31</td>
</tr>
<tr>
<td>$V_{t0,pmos}$(V)</td>
<td>-0.25</td>
<td>-0.25</td>
</tr>
</tbody>
</table>

**RESULTS AND DISCUSSION**
The proposed SRAM cells have been compared based on the FinFET and CMOS technology. The comparison includes the power consumption, static noise margin, and read access time.

**Power Consumption**

The results of the HSPICE simulations for the power consumption are depicted. The result shows that the power consumption for the SRAM FinFET is found to be less than that of the CMOS.

Table 2: **Results for CMOS and FinFET SRAM**

<table>
<thead>
<tr>
<th>Design</th>
<th>Power consumption (W)</th>
<th>Power Dissipation (W)</th>
<th>Static Read Margin (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>28.22u</td>
<td>16.1381u</td>
<td>250</td>
</tr>
<tr>
<td>FinFET (1 fin)</td>
<td>1.0293u</td>
<td>854.9901n</td>
<td>179</td>
</tr>
<tr>
<td>FinFET (2 fins)</td>
<td>667.36n</td>
<td>281.8542n</td>
<td>260</td>
</tr>
</tbody>
</table>

**HSPICE Simulation results for SRAM**
Waveforms for Read and write operations

CONCLUSION

A low-power and robust 6T SRAM cells based on FinFET has been proposed in this work. The proposed cells include the applications of the $V_t$-control method to different transistors along with the use of the built-in feedback in the cell. The HSPICE simulations for the 32nm and 45nm technologies were used to determine the efficiency of the cells. Compared to the previous work on CMOS SRAM, the proposed scheme had very low power consumption and read access time with better Static Noise Margin.

REFERENCES


